S P E C I F I C A T I O N

Passive Matrix LCD Module

(1 2 8 x 6 4 Dots)

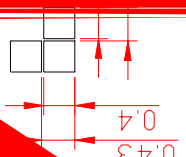
APPROVED BY

MODEL NO.

2003-06-13

CONTENTS

1.LCD TYPE: STN POSITIVE,TRANSFLECTIVE,Y-G



20

1 OF 1

UNIT: mm

3.Er

6.Mechanical Specifications

7.Electrical Specifications

7-1.Absolute Maximum Ratings

Item		Value		

7-2.Electrical Characteristics

Vdd=+5V±10%,Vss=0V, Ta=0ºC --50ºC

Item		Symbol	Spec.Value			Unit	Condition
			Min.	Typ.	Max.		
Supply Voltage	Logic	VDD-Vss	4.5	5.0	5.5	V	-
	LCD	VDD-V0	-	9.1	-	V	Ta=-20ºC !="0, #=0
			8.6	8.8	9.0	V	Ta=25ºC !="0, #=0
			-	8.6	-	V	Ta=70ºC !="0, #=0
Supply Current	Logic	IDD	-	2.0	2.5	mA	VDD=+5V±10% Vss=0V Ta=25ºC
	LCD	Io	-	1.0	1.5	mA	
Power Consumption		PD	-	500	-	mW	
Input Voltage "HIGH" Level		VIH	2.2	-	VDD	V	-
Input Voltage "LOW" Level		VIL	-0.3	-	0.6	V	-
Output Voltage "HIGH" Level		VOH	2.4	-	-	V	-
Output Voltage "LOW" Level		VOL	-	-	0.4	V	-

8.Characteristics of Backlighting(LED Unit)

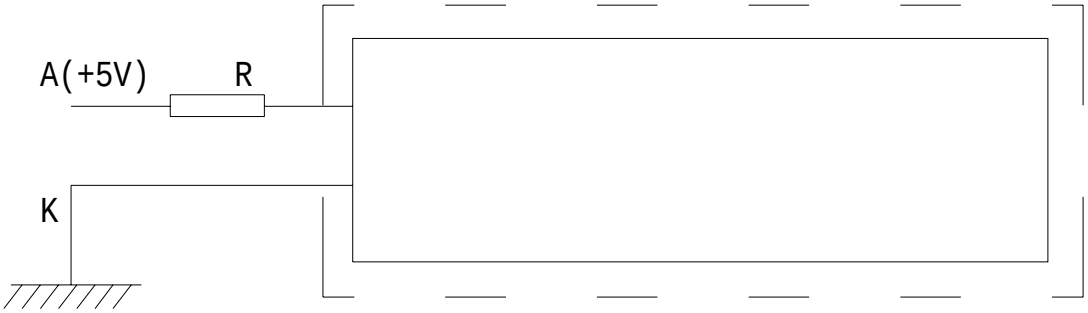
8-1.Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit.
Forward Current	IF	Ta=25ºC	-	-	mA
Reverse Voltage	VR	Ta=25ºC	-	5.0	V
Power Dissipation	PD	Ta=25ºC	-	-	mW

8-2.Opto-electric Characteristics

Item	Symbol	Comdition	Min.	Typ.	Max.	Unit
Forwars Voltage	V_F	Ta=25°C	3.7	3.9	4.1	V
Luminous	-	IF-80mA		-	-	Cd/m^2

8-3.LED Circuit Diagram



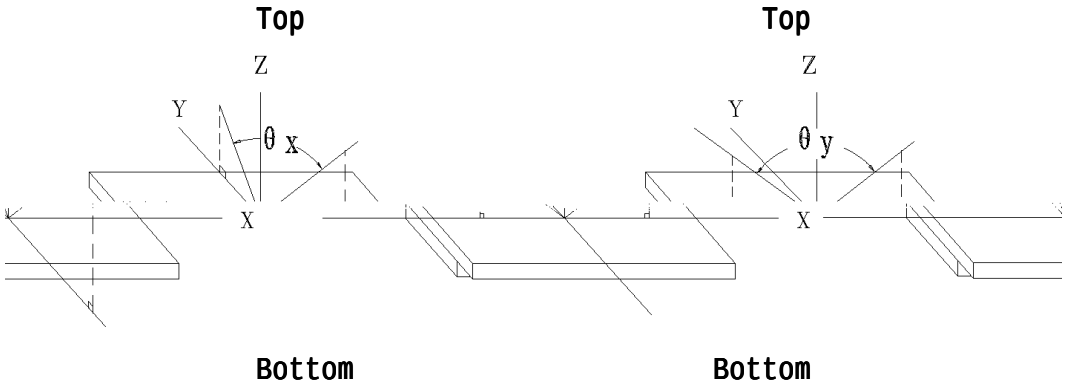
9.Electro-Optical Characteristics

9.1 Optical Characteristics

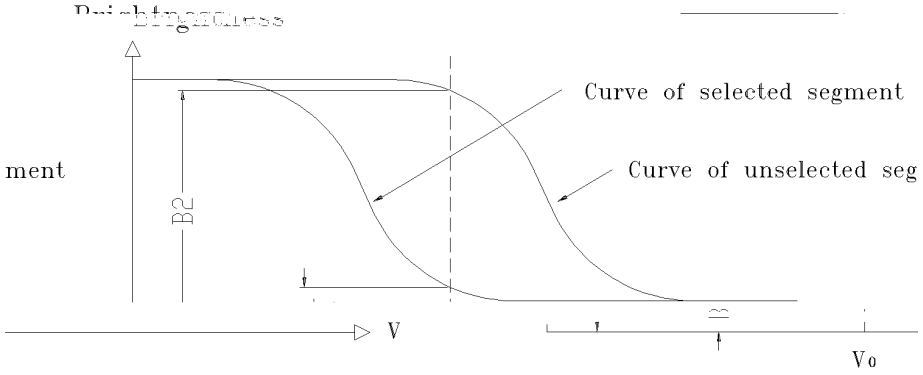
Ta=25 !

Item		Symbol	Condition		Min.	Typ.	Max.	Unit
Viewing Angle		'x	Cr$2	'y=0#	-35 -- 20			Deg
		'y		'x=0#	-30 -- 30			
Contrast Ratio		Cr	'x=0# 'y=0#		4	-	-	
Respons e Time	Turn on	Ton	'x=0# 'y=0#		-	-	250	ms
	Turn off	Toff			-	-	250	

9.2 Definition of Viewing Angle



9.3 Definition of Contrast Ratio

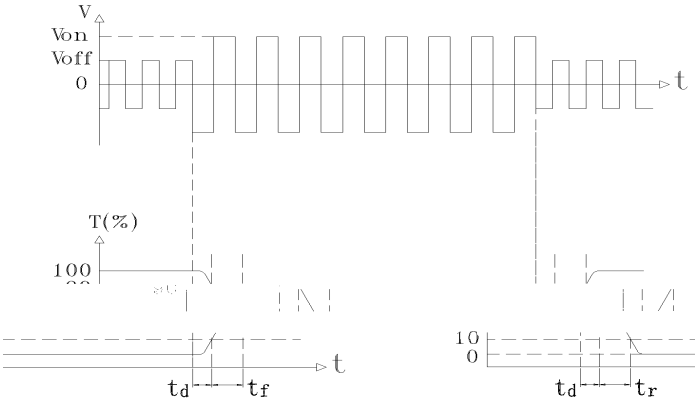


$$\text{Contrast Ratio} = B2/B1 = \frac{\text{unselected state brightness}}{\text{selected state brightness}}$$

Measuring Conditions:

1) Frame frequency: 100.0Hz

9.4 Definition of Response time



Turn on time: $t_{on} = t_d + t_r$ **Turn off time: $t_{off} = t_d + t_f$**

Measuring Condition:

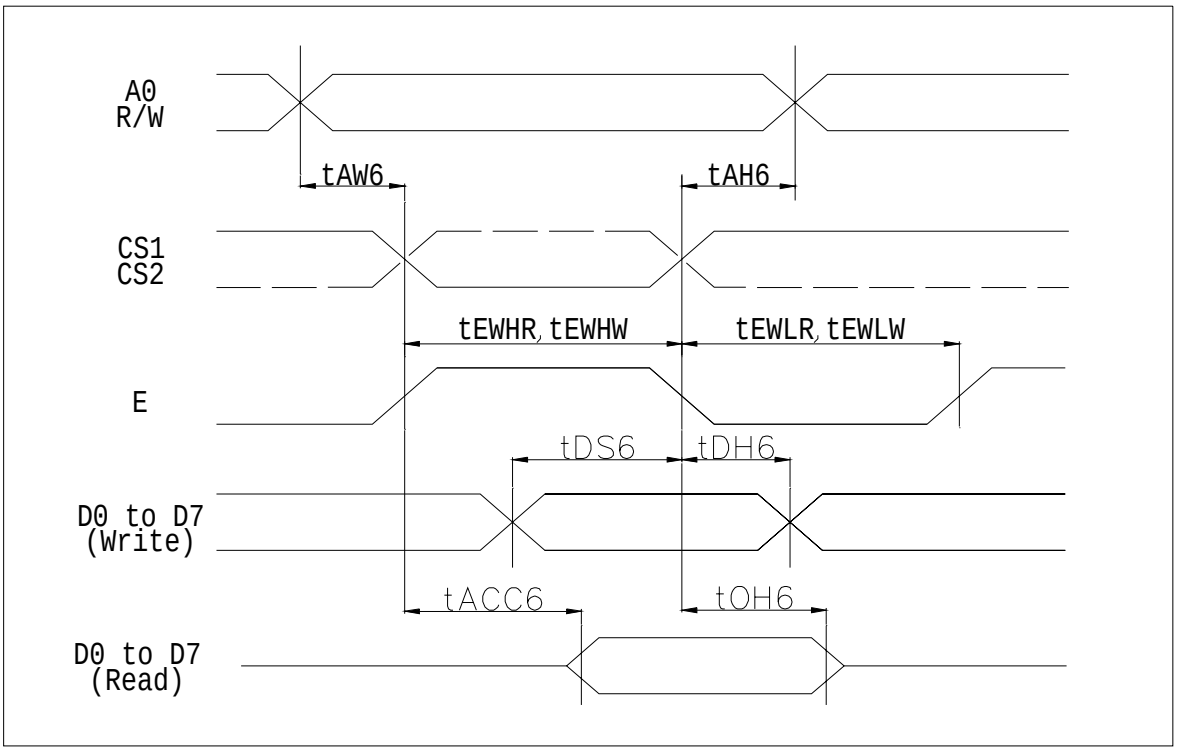
1) Operating Voltage: 6.5V **2) Frame frequency: 100.0Hz**

10.Pin Assignment

Pin No.	Symbol	Level	Function
1	V**DD**(Vcc)	+5V	Logic Supply Voltage
2	Vss(GND)	0V	Ground
3	V0	/	
4	DB0	H/L	Data Bus Line
5	DB1	H/L	
6	DB2	H/L	
7	DB3	H/L	
8	DB4	H/L	
9	DB5	H/L	
10	DB6	H/L	
11	DB7	H/L	
12	CS0	H/L	Select Master IC
13	CS1	H/L	Select Master IC
14	RES	/	
15	R/W	H/L	H:DATA Read L:Data Write
16	RS	H/L	H:Data Input L:Instruction Input
17	E	H,H->L	Enable Signal
18	VEE	/	
19	A		Power Backlighting
20	K		

11. Timing Characteristics

(1) System Bus Read/Write Characteristics (MPU->LCD MODULE)



(VDD = 4.5 V to 5.5 V, Ta = –40 to 8 °C)

Item		Signal	Symbol	Condition	Rating		Units
					Min	Max	
Address hold time		A0	tAH6		0	—	ns
Address setup time			tAW6		0	—	ns
System cycle time		A0	tCYC6		7254	—	ns
Data setup time		D0 to D7	tDS6		25	—	ns
Data hold time			tDH6		0	—	ns
Access time			tACC6	CL =	—	170	ns
Output disable time			tOH6	100 pF	10	130	ns
Enable pulse width	Read	E	tEWHR		2260	—	ns
	Write		tEWHW		1980	—	ns
Enable pulse width	Read	E	tEWLR		104	—	ns
	Write		tEWLW		7150	—	ns

12.Instruction Set

The KS0108 chip identify the data bus signals by a combination of D/I, R/W, E signals. Command interpretation and execution does not depend on the external clock, but rather is performed through internal timing only.

The interface is placed in a read mode when an “H” signal is input to the R/W terminal and placed in a write mode when a “L” signal is input to the R/W terminal and then the command is launched by inputting a high pulse to the E terminal. (See Timing Characteristics” regarding the timing.)

(1). Display ON/OFF

The display data appears when D is 1 and disappears when D is 0. Though the data is not on the screen with D = 0, it remains in the display data RAM. Therefore, you can make it appear by changing D = 0 into D = 1.

R/W	D/I	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	0	0	0	1	1	1	1	1	0	**Display OFF**
									1	**Display ON**

(2) Display Start Line

Z address D5 - D0 (binary) of the display data RAM is set in the display start line register and is displayed at the top of the screen.

		D7	D6	D5	D4	D3	D2	D1	D0	Line address
0	0	1	1	0	0	0	0	0	0	0
				0	0	0	0	0	1	1
				0	0	0	0	1	0	2
								↓		↓
				1	1	1	1	1	0	62
				1	1	1	1	1	1	63

(3) Set Page (X Address)

X address D2 –D0 (binary) of the display data RAM is set in the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

R/W	D/I	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	0	1	0	1	1	1	0	0	0	0
							0	0	1	1
								↓		↓
							1	1	0	6
							1	1	1	7

(4) Set Y Address

Y address D5 - D0 (binary) of the display data RAM is set in the Y address counter. After that, Y address counter is increased by 1 every time the data is written or read to or from MPU.

R/W	D/I	D7 D6 D5 D4 D3 D2 D1 D0	Y address
0	0	0 1 0 0 0 0 0 0	0
		0 0 0 0 0 1	1
		0 0 0 0 1 0	2
		↓	↓
		1 1 1 1 1 0	62
		1 1 1 1 1 1	63

(5) Status Read

R/W	D/I	D7	D6	D5	D4	D3 D2 D1 D0
1	0	BUSY	0	ON/OFF	RESET	0 0 0 0

BUSY	When busy is 1, the LSI is executing internal operations. No instructions are accepted while busy is 1, so you should make sure that busy is 0 before writing the next instruction.
ON/OFF	Shows the liquid crystal display conditions: on condition or off condition. When on/off is 1, the display is in off condition. When on/off is 0, the display is in on condition.
RESET	RESET = 1 shows that the system is being initialized. In this condition, no instructions except status read can be accepted. RESET = 0 shows that initializing has finished and the system is in the usual operation condition.

(6) Write Display Data

Writes 8-bit data D7 – D0 (binary) into the display data RAM. Then Y address is increased by 1 automatically.

R/W	D/I	D7 D6 D5 D4 D3 D2 D1 D0
1	0	Write data

(7) Read Display Data

Reads out 8-bit data D7 – D0 (binary) from the display data RAM. Then Y address is increased by 1 automatically.

R/W	D/I	D7 D6 D5 D4 D3 D2 D1 D0
1	0	Read data

Instructions	Command Code		Functions
	R/W D/I	D7 D6 D5 D4 D3 D2 D1 D0	
(1) Display ON/OFF	0 0	0 0 1 1 1 1 1 0 1	LCD display ON/OFF 1: ON, 0: OFF
(2) Display start line	0 0	1 1 Display start line (0-63)	Specifies the RAM line displayed at the top of the screen.
(3) Set page (X address	0 0	1 0 1 1 1 Page (0-7)	Sets the page (X address) of RAM at the page (X address) register.
(4) Set Y address	0 0	0 1 Y address (0-63)	Sets the Y address in the Y address counter.
(5) Status read	1 0	busy 0 on/off res 0 0 0 0	Reads the status. RESET 1: Reset 0: Normal ON/ OFF 1: Display off 0: Display on Busy 1: Internal operation 0: Ready
(6) Write Display data	0 1	Write data	Writes data DB0 (LSB) to DB7 (MSB) on the data bus into display RAM
(7) Read Display data	1 1	Read data	Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.

Note: Busy time varies with the frequency (f CLK) of ø1, and ø2. (1/ f CLK <= T busy <= 3/ f CLK)